

Amendments to the Specification:

Please amend paragraphs 69-108 as follows:

FIG. 2 is a cross-sectional view taken along line A-A' of FIG. 1; and

FIG. 3 is an equivalent circuit diagram of FIG. 1; ;

FIG. 4 is a plan view of an LCD device according to a first embodiment
of the present invention;

FIG. 5 is an equivalent circuit diagram of FIG. 4;

FIG. 6 is a block diagram of a gate driver driving a gate line of an LCD
device according to the first embodiment of the present invention;

FIG. 7 is a timing view of a gate pulse clock signal applied to the gate
driver of FIG. 6, and a signal output from the gate driver and applied to each
gate line;

FIG. 8 is a block diagram of a gate driver driving a gate line of an LCD
device according to the second embodiment of the present invention;

FIG. 9 is a timing view of a gate pulse clock signal and an output signal
applied to the gate driver according to the second and third embodiments of
the present invention;

FIG. 10 is a circuit diagram of a gate driver driving a gate line in an
LCD device according to the third embodiment of the present invention;

FIG. 11 is a truth table illustrating that a gate line is selectively driven
according to a clock signal when driving a gate line of an LCD device
according to the second and third embodiments of the present invention; and

FIG. 12 is a timing view illustrating that an output of a gate driver is
provided in a time-divided manner when applying one pair of gate lines of an
LCD device according to the second and third embodiments of the present
invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the preferred embodiments of
the present invention, examples of which are illustrated in the accompanying

drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

Hereinafter, an LCD device according to embodiments of the present invention will be described with reference to the accompanying drawings.

FIG. 4 is a plan view of an LCD device according to a first embodiment of the present invention. As shown in FIG. 4, in the In a first embodiment of an LCD device according to the present invention, data is provided in a time-divided manner to left and right side pixels of one data line. That is, the LCD device according to the embodiment shown includes a plurality of pairs of gate lines, each pair of gate lines including first and second gate lines 21 and 22 adjacent to each other, and a plurality of data lines 23 perpendicular to the respective gate lines 21 and 22, thereby defining the respective left and right side pixel regions. A right side pixel electrode 24a is formed in the right side pixel region and is driven by the first gate line 21. A left side pixel electrode 24b is formed in the left side pixel region and is driven by the second gate line 22.

The first and second gate lines 21 and 22 are perpendicular to the data lines, and first and second thin film transistors TFT1 and TFT2 respectively drive the right and left side pixel regions corresponding to one data line. Also, the right side pixel electrode 24a, driven by the first thin film transistor TFT1 on the first gate line 21b, is overlapped with a first pair (pair of preceding gate lines) of the first and second gate lines 21a and 22a, thereby forming first and second storage capacitors 201 and 202. In addition, the left side pixel electrode 24b, driven by the second thin film transistor TFT2 on the second gate line 22b, is overlapped with the second gate line 22a of the first pair, and the first gate line of a second pair (pair of corresponding gate lines). In this case, each gate line 21a, 22a or 22a, 21b serves as one electrode of each storage capacitor 201, 202, 203 and 204, which is not the driving gate line 21b and 22b of each pixel region but the most adjacent gate line of the corresponding pixel region.

FIG. 5 is in an equivalent circuit diagram of the LCD device of FIG. 4.
Referring to FIG. 5 illustrating the circuit diagram of the LCD device according
to the present invention the first embodiment, the number of gate lines is
doubled as compared with the number of gate lines in the LCD device
according to the related art. Meanwhile, the number of data lines is reduced
to half.

In the right side pixel region of the data line 23, a drain electrode 23b of
the first thin film transistor TFT1 is overlapped with the first and second gate
lines 21a and 22a of the first pair, so that the first and second storage
capacitors 201 and 202 are formed in parallel. In the left side pixel region of
the data line 23, the third and fourth storage capacitors 203 and 204 are
respectively interposed among the drain electrode 23b of the second thin film
transistor TFT2, the second gate line 22a of the first pair, and the first gate
line 21b of the second pair. At this time, the third and fourth storage
capacitors 203 and 204 are formed in parallel. Thus, it is possible to obtain
greater storage capacitance using the above embodiment than the related art
method for forming the storage capacitor with the preceding gate method.
Also, the method according to the above embodiment permits a reduction in
each gate line width.

In the LCD device according to the above embodiment, the plurality of
pairs of gate lines including the first and second gate lines 21 and 22
respectively cross the plurality of data line 23, thereby forming the two pixel
regions at the respective crossing points. Also, the first and second thin film
transistors TFT1 and TFT2 are formed in each pixel region. The first and
second thin film transistors TFT1 and TFT2 are driven by scanning signals
applied to the respective first and second gate lines 21 and 22. A liquid
crystal capacitor CLC is formed between a common voltage applying line and
the drain electrode of the first and second thin film transistors TFT1 and TFT2.

If the LCD device is formed according to the above embodiment in an
XGA class display (1024×768), the left and right side pixel regions of one
data line are driven according to one pair of gate lines. Such a display uses

1536 (1024×3/2) data lines and 1536 (768×2) gate lines. On comparing the LCD device according to the above embodiment with the related art LCD device having the same resolution, the number of data lines is halved and the number of gate lines is doubled.

When driving one frame, two sub-pixels (one main pixel is formed of the sub-pixels of R, G and B) are formed at crossing points between one pair of gate lines and one data line, so that a switching operation is performed for 1536×768×2 sub-pixels. At this time, each data line sequentially responds to the signal applied to the adjacent pair of gate lines, whereby the data voltage is charged in the right and left sub-pixels in order, thereby displaying a picture image.

Although not shown, in the pixel structure of the LCD device shown in FIG. 4 and 5 according According to another embodiment of the present invention, it is possible to change the right and left side pixel structure of one data line. That is, the data voltage is charged in the left and right sub-pixels in order, thereby displaying a picture image. That is, the LCD device according to another embodiment of the present invention includes a plurality of pairs of gate lines including first and second gate lines 21 and 22 adjacent to each other and a plurality of data lines 23 perpendicular to the pairs of the gate lines, for defining a plurality of pixel regions. Each left side pixel electrode (not shown) is formed in each left side pixel region for being driven by the first gate line 21. Each right side pixel electrode (not shown) is formed in each right side pixel region for being driven by the second gate line 22.

At this time, the left side pixel electrode is overlapped with the first and second of a first pair (pair of preceding gate lines), thereby forming first and second storage capacitors. Also, the right side pixel electrode is overlapped with the second gate line of the first pair, and the first gate line of a second pair (pair of corresponding gate lines), thereby forming third and fourth storage capacitors.

As mentioned above, a driving method of the LCD device according to the present invention, in which one data line is corresponding to one pair of

gate lines, will be described with reference to the accompanying drawings.

FIG. 6 is a block diagram of a gate drive driving a gate line of an LCD device according to the first embodiment of the present invention. FIG. 7 is a timing view of a gate pulse clock signal applied to the gate driver of FIG. 6, and a signal output from the gate driver and applied to each gate line.

As shown in FIG. 6 and FIG. 7, in the LCD device according to the first embodiment of the present invention, a gate driver 50 includes one or more gate drive ICs 51 driven by gate pulse clock signals HC. In a selection block of a scanning signal G1, G2, ... output from the gate drive IC 51 in the LCD device according to the first embodiment, a pulse width of the scanning signal is 1/2 that of the related art LCD device having the same resolution. For example, if a picture is transmitted at 60Hz (that is, a cycle of one frame is about 16.7msec), if the LCD device is formed according to the first embodiment in an XGA class display having a resolution of 1024×768, there are 1536 data lines (512×3: each pixel R, G and B) and 1536 gate lines on an LCD panel of a display part. That is, the selection block Ts of the scanning signal G1, G2, ... applied to each gate line is about 10.85μs(16.7msec/1536).

Accordingly, in the related art LCD device having the same resolution as that of the LCD device according to the first embodiment, the gate pulse clock signal HC having the pulse width of 21.7μs is applied to the 768 gate lines.

Meanwhile, in the LCD device according to the first embodiment, the selection block of the scanning signal applied to each gate line is about 10.85μs.

In the LCD device according to the first embodiment of the present invention, the number of the gate drive ICs 51 is doubled since the number of the gate lines is doubled. For example, if one gate drive IC 51 has 256 output pins, the LCD device uses 6 (1536/256) gate drive ICs 51.

FIG. 8 is a block diagram of a gate driver driving a gate line of an LCD device according to the second embodiment of the present invention. FIG. 9 is a timing view of a gate pulse clock signal and an output signal applied to

the gate driver according to the second or third embodiment of the present invention.

Referring to FIG. 8, a A gate driver of an LCD device according to the second embodiment of the present invention includes a gate drive IC 70 outputting a scanning signal GD1, GD2, ... to each pair of gate lines, and switching parts T1 and T2 turned-on by first and second clock signals HC1 and HC2 applied from a system, for respectively applying signals G1, G2, G3, G4, ... time-divided from the scanning signals GD1, GD2, ... to the first and second gate lines of each pair.

The gate driver of the LCD device according to the second embodiment of the present invention includes the two switching parts T1 and T2 in each output terminal of the gate drive IC 70, so that it is possible to apply the gate signal G1, G2, G3, G4, ... time-divided from the scanning signal GD1, GD2, ... output from the gate drive IC 70. Unlike the LCD device according to the first embodiment of the present invention, in the LCD device according to the second embodiment of the present invention, it is possible to apply the gate signals G1, G2, G3, G4, ... to the gate lines which are twice as many as those in the related art LCD device, with the gate drive ICs 70 corresponding to those in the related art LCD device having the same resolution.

That is, if the LCD device according to the second embodiment in which a picture is transmitted at 60Hz (a cycle of one frame is about 16.7msec) and the resolution is XGA class (1024×768), the gate driver of the LCD device according to the second embodiment of the present invention includes the three gate drive ICs 70, each having 256 output pins. At this time, each scanning signal GD1, GD2, ... output from each gate drive IC 70 has a selection block of 21.7μs. Accordingly, even though the number of the gate drive ICs 70 in the LCD device according to the second embodiment of the present invention corresponds to the number of the gate drive ICs in the LCD device according to the related art, it is possible to apply the gate signals

to twice as many gate lines as those in the related art LCD device, thereby realizing a resolution corresponding to that of the related art LCD device.

In the gate driver of the LCD device according to the second embodiment of the present invention, each output terminal of the gate drive IC 70 is divided into two parallel lines. Also, each of the first and second clock signals HC1 and HC2 has 1/2 cycle of gate shift clock, and the first and second clock signals have a phase difference at 180°. The two lines of the output terminal respectively have the first and second switching parts T1 and T2. The first and second clock signals HC1 and HC2 are respectively applied to the first and second switching parts T1 and T2, so that the first and second switching parts T1 and T2 apply the gate signal G1, G2, G3, G4, ... to each gate line. That is, the Pre-half gate signal G1, G3, G5, ... of the scanning signal GD1, GD2, GD3, ... is applied to the first gate line, and the Post-half gate signal G2, G4, G6, ... of the scanning signal GD1, GD2, GD3, ... is applied to the second gate line.

As shown in FIG. 10, for ~~For~~ outputting the scanning signal GD1, GD2, ... in the gate drive IC 70, the gate shift clock has a pulse width of 21.7 μ s, and each of the first and second clock signals HC1 and HC2, having 1/2 cycle of the gate shift clock HC, has a pulse width of 10.85 μ s. Also, each gate line G1, G2, G3, ... has a selection block during each high level of the first and second clock signals HC1 and HC2.

Hereinafter, a driving method of the gate line by using the gate driver of the LCD device according to the second embodiment of the present invention will be described as follows.

When the first scanning signal GD1 is output from the gate drive IC 70, the first gate signal G1 is applied to the first gate line when the first clock signal HC1 is high. Subsequently, the second gate signal G2 is applied to the second gate line when the second clock signal HC2 is high. Thus, even though the gate lines of the LCD device according to the second embodiment are twice as many as those in the LCD device according to the related art, the

selection block of the signal applied to each gate line is about $10.85\mu s$ in the LCD device according to the second embodiment, which is the half of the selection block of the scanning signal GD1, GD2, ... so that the LCD device spends the same time in scanning the first gate line to the last gate line in each frame as that according to the related art. Examples of the waveforms for the various signals are shown in FIG. 9.

FIG. 10 is a circuit diagram of a gate driver driving a gate line in an LCD device according to the third embodiment of the present invention. As shown in FIG. 10, the An LCD device according to the third embodiment of the present invention includes a gate drive IC 70, and AND gates AND1 and AND2. At this time, the gate drive IC outputs a scanning signal GD1, GD2, ... to each pair of gate lines. Also, the AND gates AND1 and AND2 selectively receive and logically combine first and second clock signals HC1 and HC2, and the scanning signal GD1, GD2, ..., and then apply a gate signal G1, G2, G3, G4, ... time-divided from the scanning signal GD1, GD2, ... to first and second gate lines of each pair.

In the LCD device according to the third embodiment of the present invention, a gate driver includes the two AND gates AND1 and AND2 in each output terminal of the gate drive IC 70. Also, the scanning signal GD1, GD2, ... output from the gate drive IC 70 is time-divided into two and then respectively output to the first and second gate lines. Unlike the LCD device according to the first embodiment of the present invention, in the LCD device according to the third embodiment of the present invention, it is possible to apply the signals to twice as many gate lines as those in the related art LCD device, with the number of the gate drive ICs 70 corresponding to that of the related art LCD device.

As before, if a picture is transmitted at 60Hz (a cycle of one frame is about 16.7msec), and the LCD device according to the third embodiment of the present invention has a resolution of an XGA class display (1024×768), three gate drive ICs are used, each gate drive IC having 256 output pins.

Each gate drive IC 70 outputs the scanning signal GD1, GD2, GD3, ... having a pulse width of $21.7\mu s$. The gate drive IC of the third embodiment has the same output as that of the gate drive IC in the related art LCD device having the same resolution.

Each output terminal of the gate drive IC 70 is divided into two parallel lines. Also, the first gate line includes the first AND gate AND1 for receiving and logically combining the first clock signal HC1 having a 1/2 cycle of the gate shift clock having the pulse width of $21.7\mu s$, and the scanning signal GD1, GD2, ... which is the output signal of the gate drive IC 70. The second gate line includes the second AND gate AND2 for receiving and logically combining the second clock signal HC2 having a phase difference of 180° with respect to the first clock signal HC1, and the scanning signal GD1, GD2, ..., then the logically combined value is output. Thus, the scanning signal G1, G2, G3, G4, ..., Gn is provided to the first and second gate lines of each pair in a time-divided manner.

Even though there are twice as many gate lines of the LCD device according to the third embodiment as those in the LCD device according to the related art, a selection block of the signal applied to each gate line is the half of that according to the related art, so that the LCD device spends the same time in scanning the first gate line to the last gate line at each frame as that according to the related art.

FIG. 11 is a A truth table illustrating that a gate line is selectively driven according to a clock signal when driving a gate line of an LCD device according to the second and third embodiments of the present invention; and
FIG. 12 is a timing view illustrating that an output of a gate driver is provided in a time-divided manner when applying one pair of gate lines of an LCD device according to the second and third embodiments of the present invention.

As shown in FIG. 11, in the gate driver according to the second and third embodiments of the present invention, shows that the gate signal $G_1, G_3, \dots, G_{2n-1}$ time-divided from the scanning signal GD_1, GD_2, \dots, GD_n output from the gate drive IC 70 is applied as the first gate line signal at the high level of the first clock signal HC1, and the gate signal G_2, G_4, \dots, G_{2n} is applied as the second gate line signal at the high level of the second clock signal. At this time, the wave applied to each gate line is shown in FIG. 12.